REMARKS

A request to correct the drawings is enclosed with this response. Claims 1-10 are pending in the application. Claims 7-10 have been withdrawn subject to a restriction requirement while claims 1-6 are rejected under section 103. The specification is amended to correct inconsistencies and errors of an apparent nature. These changes include revision to reference numerals at page 8 in order to effect requested corrections to the drawings. Claim 1 is amended to more clearly distinguish the invention.

The undersigned respectfully submits that the examiners restriction requirement remains an error for the reasons presented in the paper filed November 19, 2001. Specifically, the broadening of a claim by removal of a step does not result in creation of different species of that claim. Contrary to the statement made in the most recent office action it was ***not*** clearly established that the group I and group II inventions are distinct. It is requested that if the examiner still disagrees with this assessment that the examiner confer with Mr. Tom Thomas, his supervisor, to discuss the merits of this restriction requirement.

The undersigned thanks the examiner for citation of the '804 reference which forms the basis for rejecting all of the claims under section 103. However, for reasons now presented, all of the claims are fully distinguished and nonobvious over the examiner's combination of the '804 patent with the other art of record, e.g., '490,'448 and '976.

At the outset, it is noted that the '804 patent discloses more than an integrated circuit 101. Note, also, that the "electrode materials 108" are not part of the integrated

circuit 101. Nor are the output electrodes 102 part of the integrated circuit 101. The '804 reference is directed to a hybrid or composite (see abstract) that includes components in addition to an integrated circuit 101. In contrast, the claimed invention is directed to a monolithic integrated circuit device. Thus, the claimed "first and second levels of interconnect conductor" of claim 1 are portions of the claimed monolithic integrated circuit device. In contrast, none of the components cited or otherwise disclosed in the '804 patent comport with this structure. In fact, the '804 patent does not at all disclose any features of the integrated circuit 101 which would have to be relevant to the claimed invention in order to sustain the obviousness rejection.

None of the other cited art compensates for the noted deficiencies in the '804 reference. For these reasons, no combination of the cited art suggests the claimed invention. It is respectfully requested that allowance of claims 1-6 be granted.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "Version With Markings to Show Changes Made."

Respectfully,

By _____
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407-371-3250

Date: 5/22/02

Version With Markings to Show Changes Made

1) Kindly write page 1, Line 22 as follows: In particular, further reduction in area requirements for capacitors will enable further improvement in the level of integration for both digital and analog circuitry.

2) Kindly write page 1, line 21 as follows: Prior efforts to increase capacitance without increasing area consumed over a semiconductor region [where] were effected by forming multiple capacitors on separate metal levels and connecting these in parallel.

3) Kindly write page 4, line 21 as follows: A conductor runner portion 68 of metallization level 30 provides connection to the conductor plate layer 52 to provide a second connection for the capacitor formed by layers 52, 54 and 58.

4) Kindly write page 5, line 11 as follows: Generally, for the exemplary embodiments, each level of metallization is formed with an initial deposit of a dielectric layer such as the layer 70 of Figure 2 .

5) Kindly write page 5, line 13 as follows: The levels 20/30 of metallization [is] are completed prior to formation of the capacitor structure 50.

6) Kindly write page 6, line 1 as follows: For dual Damascene structures such as the illustrated levels 20/30, both the via portion (providing connection between different levels of metallization) and the conductor portion (providing conductor runners within a level of metallization) are formed in sequential pattern and etch steps, followed by deposit of the barrier layer material, a seed layer and then an

electro-deposition of the Cu to completely fill the via portions and the conductor member portions of the openings.

7) Kindly write page 6, line 11 as follows: Once the dual Damascene levels 20/30 [is] are completed the layers

8) Kindly write page 7, line 12 as follows: See next Figure 6, which illustrates a 60 nm barrier layer 80 of silicon nitride deposited on the exposed portions of layers 52, 54, 56, 58 and 60 as well as the dielectric layer 70 and exposed regions of Cu in the metallization level [20] 30.

9) Kindly write page 8, line 1 as follows: A lower conductor level 30 includes a runner portion [124] 123 effecting connection between lower plate 52 and a via portion 92 of level 40.

10) Kindly write page 8, line 8 as follows: Connections to individual layers 122 are made through via portions 126 and conductive runners, 120, 123 and [124] 125 to configure four capacitors connected in parallel.

11) Kindly amend claim 1 as follows: A monolithic integrated circuit [A semiconductor device] comprising:

at least first and second levels of interconnect conductor for connection to a semiconductor layer; and

a stack of alternating conductive and insulative layers formed in vertical alignment with respect to an underlying plane and formed between the first and second levels of conductor, including

a first conductive layer,

a first insulator layer formed over the first conductive layer,

a second conductive layer formed over the first insulative layer ,

a second insulator layer formed over the second conductive layer,

and

a third conductive layer formed over the second insulative layer,

with the first and third conductive layers commonly connected.